**ANKARA UNIVERSITY COMPUTER ENGINEERING**

**2017-2018 COM275 FINAL EXAMINATION**

**Name : January 11, 2018**

**Student No : Duration: 90 minutes**

**Section : □ A (%30) □ B (%100)**

**Part I** Answer ONLY TWO of the following questions. **(10 points for each answer)**

1. What is the difference between a latch and a flip-flop?
2. What does volatile/nonvolatile mean for memory?
3. What are the different ways to describe logic of a module using a Hardware Description Language (HDL)?

**Part II**  Answer ONLY THREE of the following questions. **(20 points for each answer)**

1. A sequential circuit with two flip-flops and , one input, ; and one output is specified by the state and output equations below.
   1. Write the state table for this circuit including the output as well as and columns.
   2. Write the input equations and draw the logic diagram of the circuit.
2. Design a 3-bit shift register with a single control input that shifts its bits to the left when and to the right when . The register will have another input which is (serial input) and an output which is (serial output).
3. Implement the following functions with a PLA. Use as few AND gates as possible. Only provide the programing table (the fuse map).
4. Draw the logic diagram of the circuit specified by the following Verilog description:

**module** MyCircuit (x, y, F);

**input** x, y;

**output** F;

**wire** a, b, c, d;

**and** #10 (c, x, b);

**and** #10 (d, y, a);

**or** #10 (F, c, d);

**not** #5 (a, x);

**not** #5 (b, y);

**endmodule**

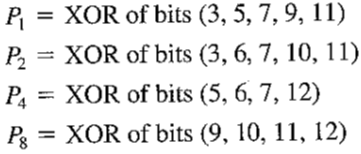
**Part III** Answer ONLY ONE of the following questions. **(20 points)**

1. Design a Mealy type Finite State Machine which reads a string of bits and recognizes when the number of 1’s is a multiple of 3. In other words, the machine will only output 1 when it sees the 3rd, 6th, 9th, … 1 in the input string. For example, if the input string is 0101111001, the output will be 0000100001. Derive the corresponding circuit using D flip-flops.
2. A circuit with two D flip flops and a single input is given below. Analyze this circuit and describe what it does.



1. The table below shows 12 bits received by a device. The bits include 4 parity bits to create Hamming code that were created with the groups shown below. Determine whether received bits contain an error. If there is an error, at which bit is it?

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Address | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| Parity | P1 | P2 |  | P4 |  |  |  | P8 |  |  |  |  |
| Received bits | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |



1. Write a simple Verilog test bench to test the circuit given in Part II Question 4.